# 74HC590

## 8-bit binary counter with output register; 3-state

Rev. 02 — 28 April 2009 Product data sheet

## 1. General description

The 74HC590 is a high-speed Si-gate CMOS device and is pin compatible with Low power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard no. 7A.

The 74HC590 is an 8-bit binary counter with a storage register and 3-state outputs. The storage register has parallel (Q0 to Q7) outputs. The binary counter features a master reset counter ($\overline{MRC}$) and count enable ($\overline{CE}$) inputs. The counter and storage register have separate positive edge triggered clock (CPC and CPR) inputs. If both clocks are connected together, the counter state always is one count ahead of the register. Internal circuitry prevents clocking from the clock enable. A ripple carry output ($\overline{RCO}$) is provided for cascading. Cascading is accomplished by connecting $\overline{RCO}$ of the first stage to $\overline{CE}$ of the second stage. Cascading for larger count chains can be accomplished by connecting $\overline{RCO}$ of each stage to the counter clock (CPC) input of the following stage. If both clocks are connected together, the counter state always is one count ahead of the register.

## 2. Features

- Counter and register have independent clock inputs
- Counter has master reset
- Complies with JEDEC standard no. 7A
- Multiple package options
- ESD protection:
  - HBM JESD22-A114E exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
  - CDM JESD22-C101C exceeds 2000 V
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

## 3. Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| 74HC590N | –40 °C to +125 °C | DIP16 | plastic dual in-line package; 16 leads (300 mil) | SOT38-4 |
| 74HC590D | –40 °C to +125 °C | SO16 | plastic small outline package; 16 leads; body width 3.9 mm | SOT109-1 |
| 74HC590PW | –40 °C to +125 °C | TSSOP16 | plastic thin shrink small outline package; 16 leads; body width 4.4 mm | SOT403-1 |
| 74HC590BQ | –40 °C to +125 °C | DHVQFN16 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body $2.5 \times 3.5 \times 0.85$ mm | SOT763-1 |

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## 4. Functional diagram

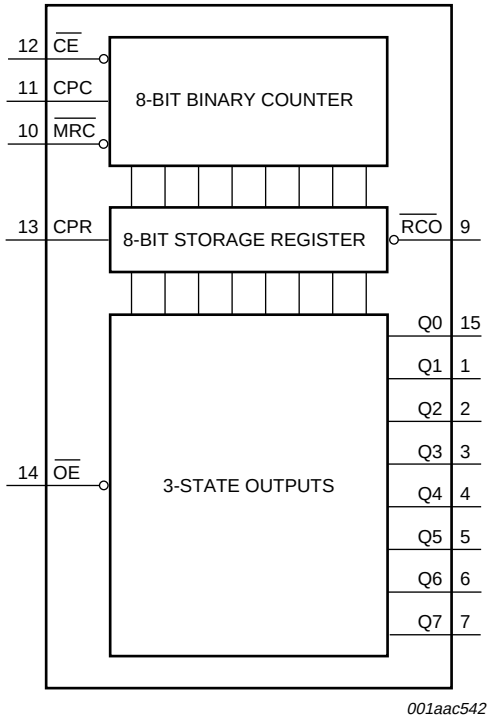



**Fig 1. Functional diagram**

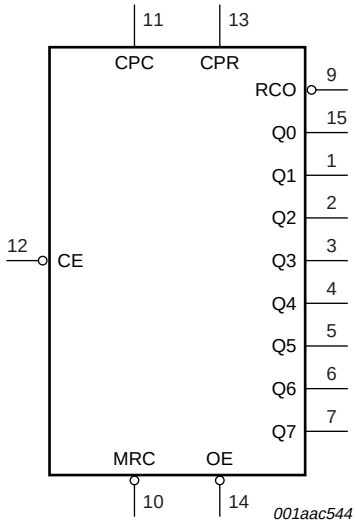



**Fig 2. Logic symbol**

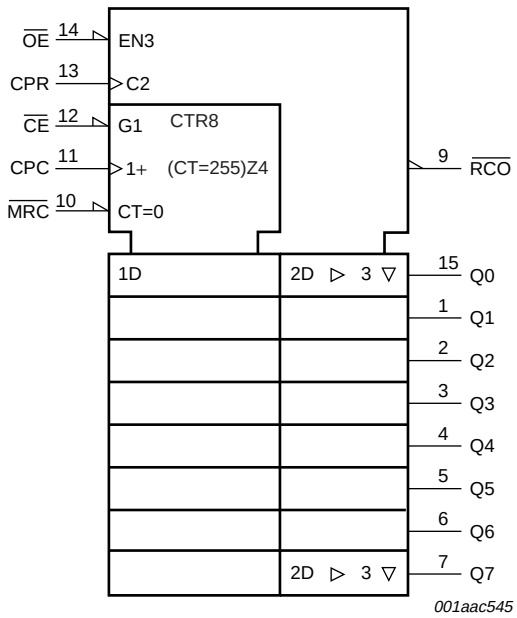



**Fig 3. IEC logic symbol**


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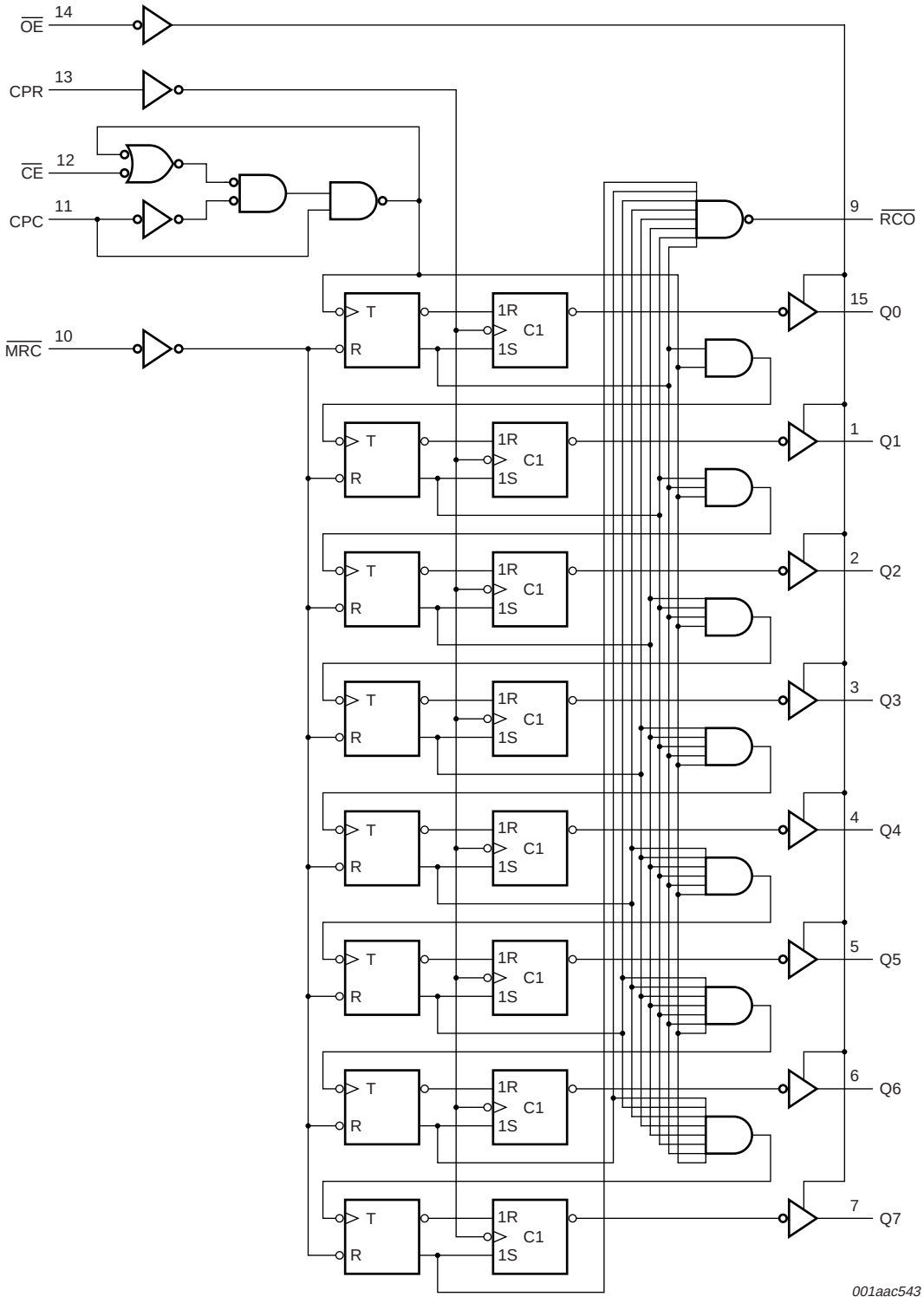



**Fig 4. Logic diagram**



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# 5. Pinning information

## 5.1 Pinning

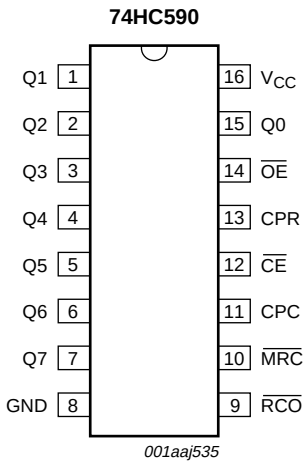



**Fig 5. Pin configuration DIP16**

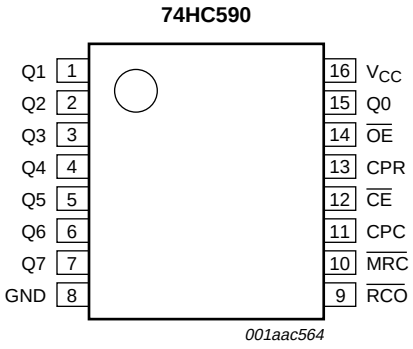
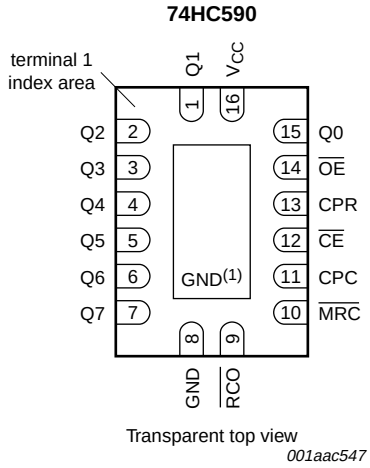



**Fig 6. Pin configuration SO16 and TSSOP16**




(1) The die substrate is attached to the exposed die pad using conductive die attach material. It can not be used as a supply pin or input.

**Fig 7. Pin configuration DHVQFN16**

## 5.2 Pin description

**Table 2. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| Q0 to Q7 | 15, 1, 2, 3, 4, 5, 6, 7 | parallel data output |
| GND | 8 | ground (0 V) |
| $\overline{RCO}$ | 9 | ripple carry output (active LOW) |
| $\overline{MRC}$ | 10 | master reset counter input (active LOW) |
| CPC | 11 | counter clock input (active HIGH) |
| $\overline{CE}$ | 12 | count enable input (active LOW) |
| CPR | 13 | register clock input (active HIGH) |
| $\overline{OE}$ | 14 | output enable input (active LOW) |
| $V_{CC}$ | 16 | supply voltage |


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## 6. Functional description

**Table 3. Function table[1] [2]**

| Inputs | | | | | Description |
|---|---|---|---|---|---|
| $\overline{OE}$ | CPR | $\overline{MRC}$ | $\overline{CE}$ | CPC | |
| H | X | X | X | X | Q outputs disable |
| L | X | X | X | X | Q outputs enable |
| X | ↑ | X | X | X | counter data stored into register |
| X | ↓ | X | X | X | register stage is not changed |
| X | X | L | X | X | counter clear |
| X | X | H | L | ↑ | advance one count |
| X | X | H | L | ↓ | no count |
| X | X | H | H | X | no count |

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care;
↑ = LOW-to-HIGH transition;
↓ = HIGH-to-LOW transition.

[2] $\overline{RCO} = \overline{Q0'} \cdot \overline{Q1'} \cdot \overline{Q2'} \cdot \overline{Q3'} \cdot \overline{Q4'} \cdot \overline{Q5'} \cdot \overline{Q6'} \cdot \overline{Q7'}$ (Q0' to Q7' are internal outputs of the counter).


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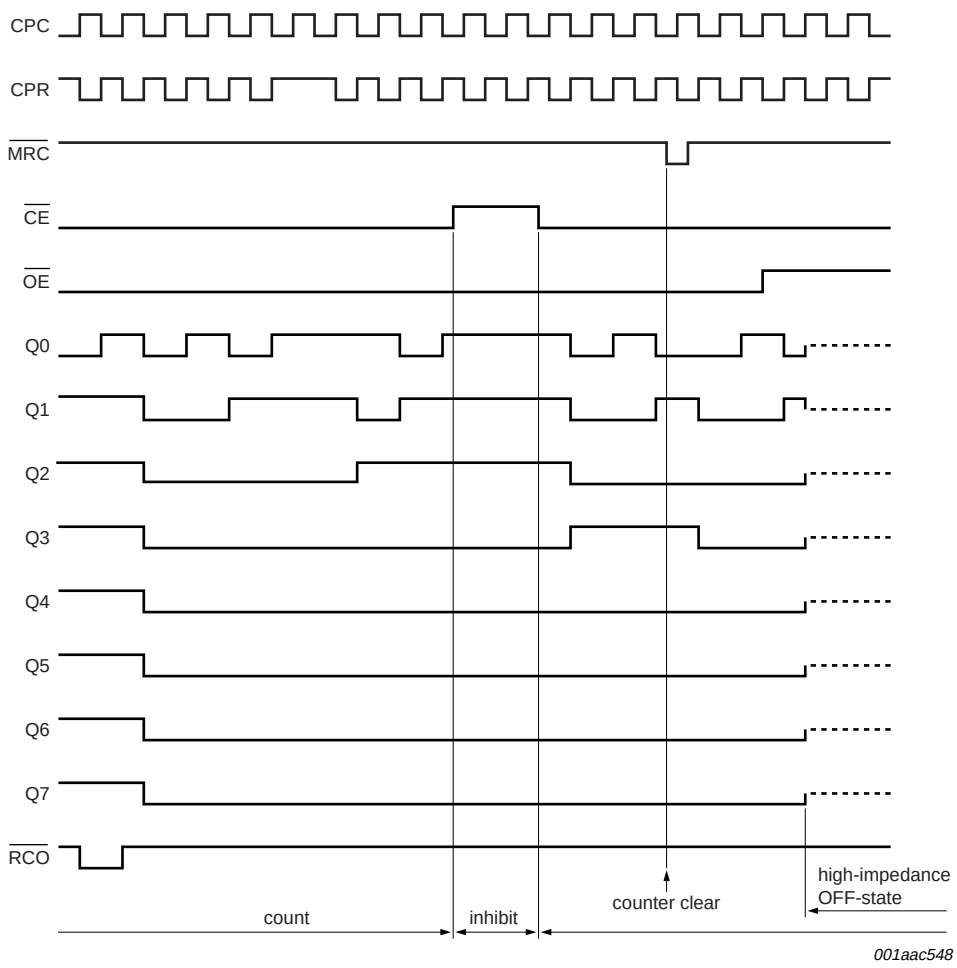



**Fig 8. Typical timing sequence**



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# 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | | –0.5 | +7.0 | V |
| $I_{IK}$ | input clamping current | $V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V | [1] | - | ±20 | mA |
| $I_{OK}$ | output clamping current | $V_O < –0.5$ V or $V_O > V_{CC} + 0.5$ V | [1] | - | ±20 | mA |
| $I_O$ | output current | $V_O = –0.5$ V to $V_{CC} + 0.5$ V | | | | |
| | | $\overline{RCO}$ standard output | | - | ±25 | mA |
| | | Qn bus driver output | | - | ±35 | mA |
| $I_{CC}$ | supply current | | | - | 70 | mA |
| $I_{GND}$ | ground current | | | –70 | - | mA |
| $T_{stg}$ | storage temperature | | | –65 | +150 | °C |
| $P_{tot}$ | total power dissipation | $T_{amb} = –40$ °C to +125 °C | [2] | | | |
| | | DIP16 package | | - | 750 | mW |
| | | SO16 package | | - | 500 | mW |
| | | TSSOP16 package | | - | 500 | mW |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For DIP16 package: $P_{tot}$ derates linearly with 12 mW/K above 70 °C.
For SO16 packages: $P_{tot}$ derates linearly with 8 mW/K above 70 °C.
For TSSOP16 packages: $P_{tot}$ derates linearly with 5.5 mW/K above 60 °C.
For DHVQFN16 packages: $P_{tot}$ derates linearly with 8 mW/K above 60 °C.

# 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | 2.0 | 5.0 | 6.0 | V |
| $V_I$ | input voltage | | 0 | - | $V_{CC}$ | V |
| $V_O$ | output voltage | | 0 | - | $V_{CC}$ | V |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC} = 2.0$ V | - | - | 625 | ns/V |
| | | $V_{CC} = 4.5$ V | - | 1.67 | 139 | ns/V |
| | | $V_{CC} = 6.0$ V | - | - | 83 | ns/V |
| $T_{amb}$ | ambient temperature | | –40 | - | +125 | °C |



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## 9. Static characteristics

**Table 6. Static characteristics**

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | 25 °C | | | –40 °C to +85 °C | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 2.0 V | 1.5 | 1.2 | - | 1.5 | - | 1.5 | - | V |
| | | $V_{CC}$ = 4.5 V | 3.15 | 2.4 | - | 3.15 | - | 3.15 | - | V |
| | | $V_{CC}$ = 6.0 V | 4.2 | 3.2 | - | 4.2 | - | 4.2 | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 2.0 V | - | 0.8 | 0.5 | - | 0.5 | - | 0.5 | V |
| | | $V_{CC}$ = 4.5 V | - | 2.1 | 1.35 | - | 1.35 | - | 1.35 | V |
| | | $V_{CC}$ = 6.0 V | - | 2.8 | 1.8 | - | 1.8 | - | 1.8 | V |
| $V_{OH}$ | HIGH-level output voltage | $V_I = V_{IH}$ or $V_{IL}$ | | | | | | | | |
| | | all outputs | | | | | | | | |
| | | $I_O$ = –20 µA; $V_{CC}$ = 2.0 V | 1.9 | 2.0 | - | 1.9 | - | 1.9 | - | V |
| | | $I_O$ = –20 µA; $V_{CC}$ = 4.5 V | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | $I_O$ = –20 µA; $V_{CC}$ = 6.0 V | 5.9 | 6.0 | - | 5.9 | - | 5.9 | - | V |
| | | $\overline{RCO}$ standard output | | | | | | | | |
| | | $I_O$ = –4 mA; $V_{CC}$ = 4.5 V | 4.18 | 4.31 | - | 4.13 | - | 4.1 | - | V |
| | | $I_O$ = –5.2 mA; $V_{CC}$ = 6.0 V | 5.68 | 5.80 | - | 5.63 | - | 5.6 | - | V |
| | | Qn bus driver output | | | | | | | | |
| | | $I_O$ = –6.0 mA; $V_{CC}$ = 4.5 V | 4.18 | 4.31 | - | 4.13 | - | 4.1 | - | V |
| | | $I_O$ = –7.8 mA; $V_{CC}$ = 6.0 V | 5.68 | 5.80 | - | 5.63 | - | 5.6 | - | V |
| $V_{OL}$ | LOW-level output voltage | $V_I = V_{IH}$ or $V_{IL}$ | | | | | | | | |
| | | all outputs | | | | | | | | |
| | | $I_O$ = 20 µA; $V_{CC}$ = 2.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 20 µA; $V_{CC}$ = 4.5 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 20 µA; $V_{CC}$ = 6.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $\overline{RCO}$ standard output | | | | | | | | |
| | | $I_O$ = 4 mA; $V_{CC}$ = 4.5 V | - | 0.17 | 0.26 | - | 0.33 | - | 0.4 | V |
| | | $I_O$ = 5.2 mA; $V_{CC}$ = 6.0 V | - | 0.18 | 0.26 | - | 0.33 | - | 0.4 | V |
| | | Qn bus driver output | | | | | | | | |
| | | $I_O$ = 6.0 mA; $V_{CC}$ = 4.5 V | - | 0.17 | 0.26 | - | 0.33 | - | 0.4 | V |
| | | $I_O$ = 7.8 mA; $V_{CC}$ = 6.0 V | - | 0.18 | 0.26 | - | 0.33 | - | 0.4 | V |
| $I_I$ | input leakage current | $V_I = V_{CC}$ or GND; $V_{CC}$ = 6.0 V | - | - | ±0.1 | - | ±1.0 | - | ±1.0 | µA |
| $I_{OZ}$ | OFF-state output current | per pin; $V_I = V_{IH}$ or $V_{IL}$; $V_O = V_{CC}$ or GND; other inputs at $V_{CC}$ or GND; $V_{CC}$ = 6.0 V | - | - | ±0.5 | - | ±5.0 | - | ±10 | µA |
| $I_{CC}$ | supply current | $V_I = V_{CC}$ or GND; $I_O$ = 0 A; $V_{CC}$ = 6.0 V | - | - | 4.0 | - | 40 | - | 80 | µA |
| $C_I$ | input capacitance | | - | 3.5 | - | - | - | - | - | pF |



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## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

*GND (ground = 0 V); for test circuit see Figure 15.*

| Symbol | Parameter | Conditions | 25 °C | | | −40 °C to +85 °C | | −40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| $t_{pd}$ | propagation delay | CPC to $\overline{RCO}$; see Figure 9 [1] | | | | | | | | |
| | | $V_{CC}$ = 2.0 V | - | 52 | 150 | - | 190 | - | 230 | ns |
| | | $V_{CC}$ = 4.5 V | - | 19 | 30 | - | 38 | - | 45 | ns |
| | | $V_{CC}$ = 6.0 V | - | 15 | 26 | - | 33 | - | 40 | ns |
| | | CPR to Qn; see Figure 10 | | | | | | | | |
| | | $V_{CC}$ = 2.0 V | - | 50 | 140 | - | 175 | - | 210 | ns |
| | | $V_{CC}$ = 4.5 V | - | 17 | 28 | - | 35 | - | 42 | ns |
| | | $V_{CC}$ = 6.0 V | - | 14 | 24 | - | 30 | - | 36 | ns |
| $t_{PLH}$ | LOW to HIGH propagation delay | $\overline{MRC}$ to $\overline{RCO}$; see Figure 11 | | | | | | | | |
| | | $V_{CC}$ = 2.0 V | - | 53 | 130 | - | 165 | - | 200 | ns |
| | | $V_{CC}$ = 4.5 V | - | 18 | 26 | - | 33 | - | 40 | ns |
| | | $V_{CC}$ = 6.0 V | - | 14 | 22 | - | 28 | - | 34 | ns |
| $t_{en}$ | enable time | $\overline{OE}$ to Qn; see Figure 12 [2] | | | | | | | | |
| | | $V_{CC}$ = 2.0 V | - | 28 | 105 | - | 130 | - | 160 | ns |
| | | $V_{CC}$ = 4.5 V | - | 13 | 21 | - | 26 | - | 32 | ns |
| | | $V_{CC}$ = 6.0 V | - | 11 | 18 | - | 22 | - | 27 | ns |
| $t_{dis}$ | disable time | $\overline{OE}$ to Qn; see Figure 12 [3] | | | | | | | | |
| | | $V_{CC}$ = 2.0 V | - | 28 | 105 | - | 130 | - | 160 | ns |
| | | $V_{CC}$ = 4.5 V | - | 13 | 21 | - | 26 | - | 32 | ns |
| | | $V_{CC}$ = 6.0 V | - | 11 | 18 | - | 22 | - | 27 | ns |
| $t_W$ | pulse width | CPC and CPR; HIGH or LOW; see Figure 9 and Figure 10 | | | | | | | | |
| | | $V_{CC}$ = 2.0 V | 100 | 24 | - | 125 | - | 145 | - | ns |
| | | $V_{CC}$ = 4.5 V | 20 | 9 | - | 25 | - | 29 | - | ns |
| | | $V_{CC}$ = 6.0 V | 17 | 8 | - | 21 | - | 25 | - | ns |
| | | $\overline{MRC}$; LOW; see Figure 11 | | | | | | | | |
| | | $V_{CC}$ = 2.0 V | 75 | 28 | - | 95 | - | 110 | - | ns |
| | | $V_{CC}$ = 4.5 V | 15 | 8 | - | 19 | - | 22 | - | ns |
| | | $V_{CC}$ = 6.0 V | 13 | 6 | - | 16 | - | 19 | - | ns |
| $t_{su}$ | set-up time | CPC to CPR; see Figure 14 | | | | | | | | |
| | | $V_{CC}$ = 2.0 V | 100 | 46 | - | 125 | - | 150 | - | ns |
| | | $V_{CC}$ = 4.5 V | 20 | 14 | - | 25 | - | 30 | - | ns |
| | | $V_{CC}$ = 6.0 V | 17 | 10 | - | 21 | - | 26 | - | ns |
| | | $\overline{CE}$ to CPC; see Figure 13 | | | | | | | | |
| | | $V_{CC}$ = 2.0 V | 100 | 44 | - | 125 | - | 150 | - | ns |
| | | $V_{CC}$ = 4.5 V | 20 | 11 | - | 25 | - | 30 | - | ns |
| | | $V_{CC}$ = 6.0 V | 17 | 9 | - | 21 | - | 26 | - | ns |



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**Table 7. Dynamic characteristics** *…continued*

*GND (ground = 0 V); for test circuit see Figure 15.*

| Symbol | Parameter | Conditions | 25 °C | | | –40 °C to +85 °C | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| $t_h$ | hold time | $\overline{CE}$ to CPC; see Figure 13 | | | | | | | | |
| | | $V_{CC}$ = 2.0 V | 0 | - | - | 0 | - | 0 | - | ns |
| | | $V_{CC}$ = 4.5 V | 0 | - | - | 0 | - | 0 | - | ns |
| | | $V_{CC}$ = 6.0 V | 0 | - | - | 0 | - | 0 | - | ns |
| $t_{rec}$ | recovery time | $\overline{MRC}$ to CPC; see Figure 11 | | | | | | | | |
| | | $V_{CC}$ = 2.0 V | 75 | 28 | - | 95 | - | 110 | - | ns |
| | | $V_{CC}$ = 4.5 V | 15 | 7 | - | 19 | - | 22 | - | ns |
| | | $V_{CC}$ = 6.0 V | 13 | 6 | - | 16 | - | 19 | - | ns |
| $f_{max}$ | maximum frequency | CPC or CPR; see Figure 9 and Figure 10 | | | | | | | | |
| | | $V_{CC}$ = 2.0 V | 6.6 | 16 | - | 5.2 | - | 4.4 | - | MHz |
| | | $V_{CC}$ = 4.5 V | 33 | 52 | - | 26 | - | 22 | - | MHz |
| | | $V_{CC}$ = 6.0 V | 39 | 61 | - | 31 | - | 26 | - | MHz |
| $C_{PD}$ | power dissipation capacitance | $V_I$ = GND to $V_{CC}$ [4] | - | 44 | - | - | - | - | - | pF |

[1] $t_{pd}$ is the same as $t_{PHL}$, $t_{PLH}$.

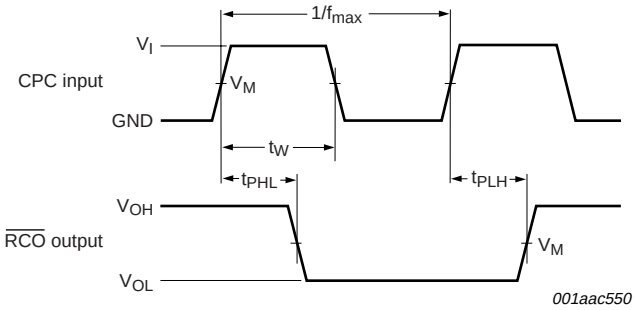
[2] $t_{en}$ is the same as $t_{PZH}$ and $t_{PZL}$.

[3] $t_{dis}$ is the same as $t_{PLZ}$ and $t_{PHZ}$.

[4] $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
$f_i$ = input frequency in MHz;
$f_o$ = output frequency in MHz;
$C_L$ = output load capacitance in pF;
$V_{CC}$ = supply voltage in V;
N = number of inputs switching;
$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.


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## 11. Waveforms



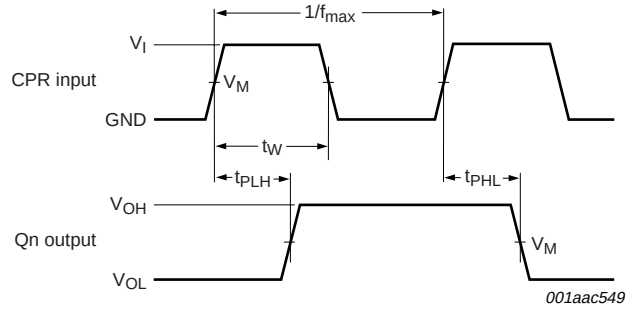

Measurement points are given in Table 8.

$V_{OL}$ and $V_{OH}$ are the typical output voltage levels that occur with the output load.

**Fig 9. Waveforms showing the propagation delays from the counter clock input (CPC) to ripple carry ($\overline{RCO}$) output and the CPC pulse width**

**Table 8. Measurement points**

| Type | Input | | Output |
|---|---|---|---|
| | $V_I$ | $V_M$ | $V_M$ |
| 74HC590 | $V_{CC}$ | $0.5V_{CC}$ | $0.5V_{CC}$ |

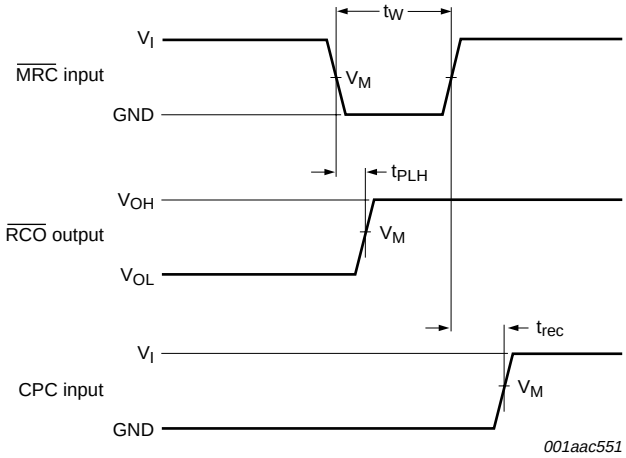



Measurement points are given in Table 8.

$V_{OL}$ and $V_{OH}$ are the typical output voltage levels that occur with the output load.

**Fig 10. Waveforms showing the propagation delays from the register clock input (CPR) to output (Qn) and the register clock pulse width**

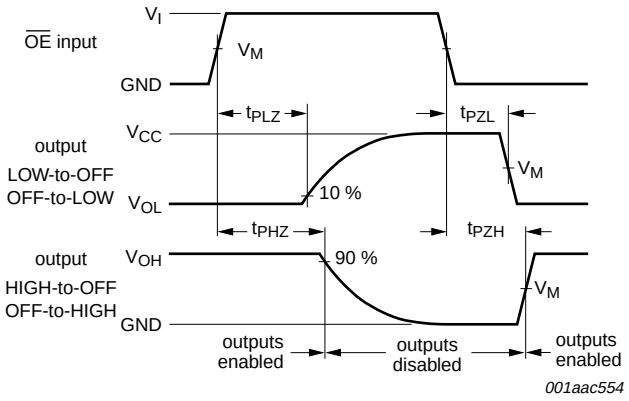

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Measurement points are given in Table 8.

$V_{OL}$ and $V_{OH}$ are the typical output voltage levels that occur with the output load.

**Fig 11. Waveforms showing the propagation delays from the master reset counter input ($\overline{MRC}$) to output ($\overline{RCO}$), the $\overline{MRC}$ pulse width and recovery time**



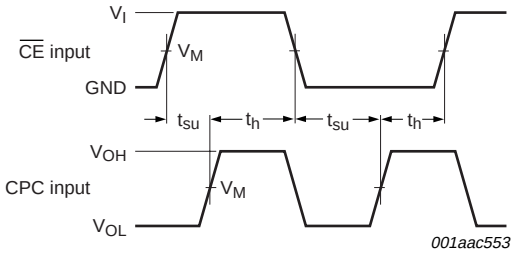

Measurement points are given in Table 8.

$V_{OL}$ and $V_{OH}$ are the typical output voltage levels that occur with the output load.

**Fig 12. Waveforms showing the 3-state enable and disable times**



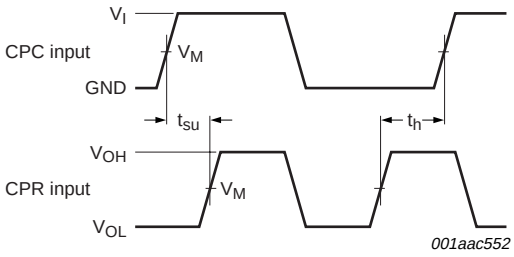
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Measurement points are given in Table 8.

$V_{OL}$ and $V_{OH}$ are the typical output voltage levels that occur with the output load.

**Fig 13. Waveforms showing the set-up and hold times for the count enable input ($\overline{CE}$) to the counter clock input (CPC)**



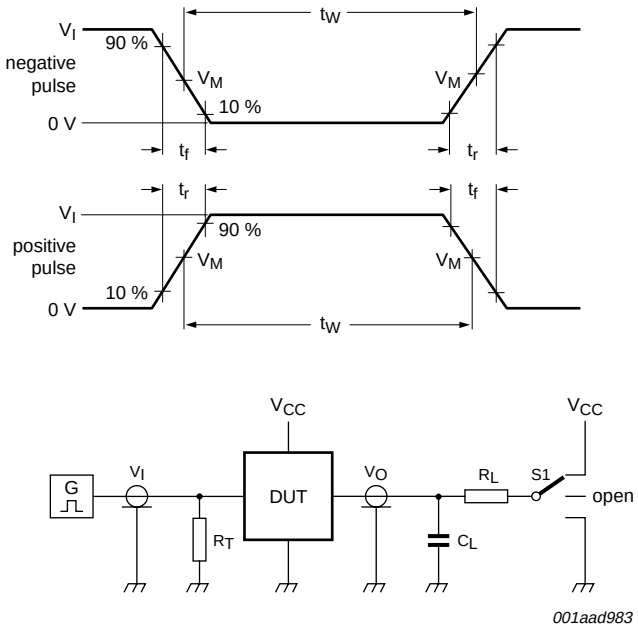

Measurement points are given in Table 8.

$V_{OL}$ and $V_{OH}$ are the typical output voltage levels that occur with the output load.

**Fig 14. Waveforms showing the set-up and hold times for the counter clock input (CPC) to the register clock input (CPR)**



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Test data is given in Table 9.

Definitions test circuit:

$R_T$ = Termination resistance should be equal to output impedance $Z_o$ of the pulse generator.

$C_L$ = Load capacitance including jig and probe capacitance.

$R_L$ = Load resistance.

S1 = Test selection switch.

**Fig 15. Test circuit for measuring switching times**

**Table 9. Test data**

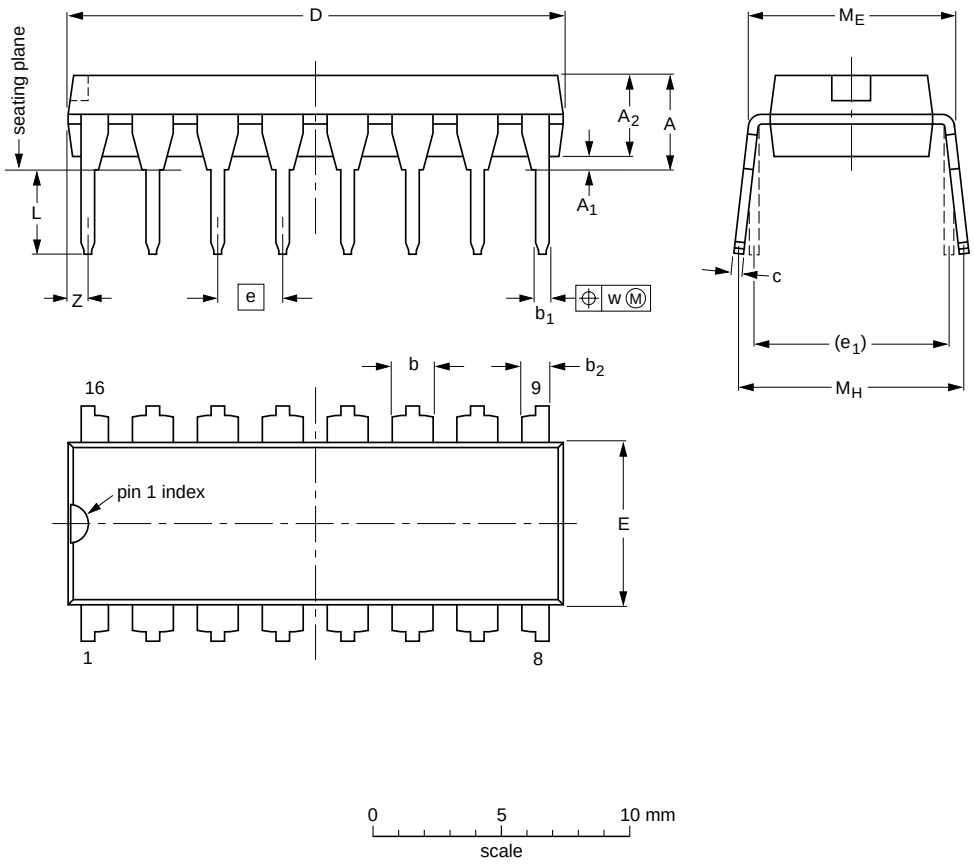
| Supply voltage | Input | | Load | | Switch position | | |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | $V_I$ | $t_r$, $t_f$ | $C_L$ | $R_L$ | $t_{PHL}$, $t_{PLH}$ | $t_{PZH}$, $t_{PHZ}$ | $t_{PZL}$, $t_{PLZ}$ |
| 2.0 V to 6.0 V | $V_{CC}$ | 6 ns | 50 pF | 1 kΩ | open | GND | $V_{CC}$ |



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## 12. Package outline

**DIP16: plastic dual in-line package; 16 leads (300 mil)** **SOT38-4**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ min. | $A_2$ max. | b | $b_1$ | $b_2$ | c | D (1) | E (1) | e | $e_1$ | L | $M_E$ | $M_H$ | w | Z (1) max. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.2 | 0.51 | 3.2 | 1.73<br>1.30 | 0.53<br>0.38 | 1.25<br>0.85 | 0.36<br>0.23 | 19.50<br>18.55 | 6.48<br>6.20 | 2.54 | 7.62 | 3.60<br>3.05 | 8.25<br>7.80 | 10.0<br>8.3 | 0.254 | 0.76 |
| inches | 0.17 | 0.02 | 0.13 | 0.068<br>0.051 | 0.021<br>0.015 | 0.049<br>0.033 | 0.014<br>0.009 | 0.77<br>0.73 | 0.26<br>0.24 | 0.1 | 0.3 | 0.14<br>0.12 | 0.32<br>0.31 | 0.39<br>0.33 | 0.01 | 0.03 |

**Note**

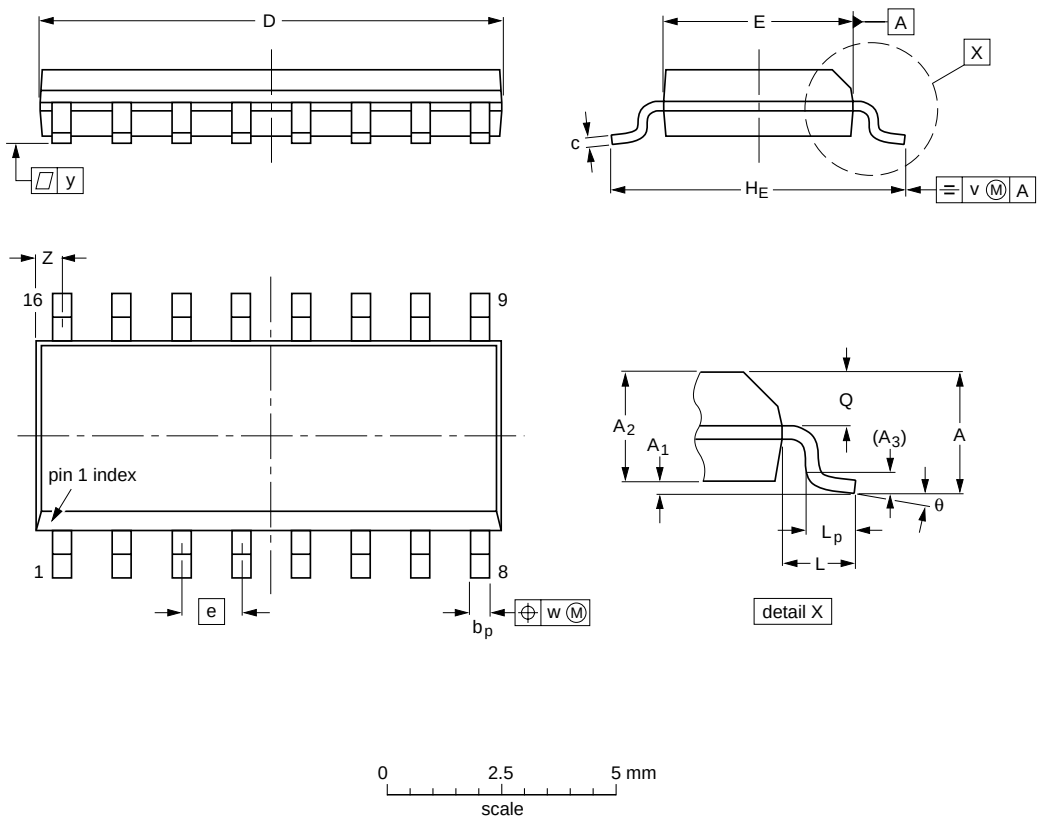
1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT38-4 | | | | | | ~~95-01-14~~<br>03-02-13 |

**Fig 16. Package outline SOT38-4 (DIP16)**


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**SO16: plastic small outline package; 16 leads; body width 3.9 mm** **SOT109-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.75 | 0.25<br>0.10 | 1.45<br>1.25 | 0.25 | 0.49<br>0.36 | 0.25<br>0.19 | 10.0<br>9.8 | 4.0<br>3.8 | 1.27 | 6.2<br>5.8 | 1.05 | 1.0<br>0.4 | 0.7<br>0.6 | 0.25 | 0.25 | 0.1 | 0.7<br>0.3 | $8^o$<br>$0^o$ |
| inches | 0.069 | 0.010<br>0.004 | 0.057<br>0.049 | 0.01 | 0.019<br>0.014 | 0.0100<br>0.0075 | 0.39<br>0.38 | 0.16<br>0.15 | 0.05 | 0.244<br>0.228 | 0.041 | 0.039<br>0.016 | 0.028<br>0.020 | 0.01 | 0.01 | 0.004 | 0.028<br>0.012 | |

**Note**

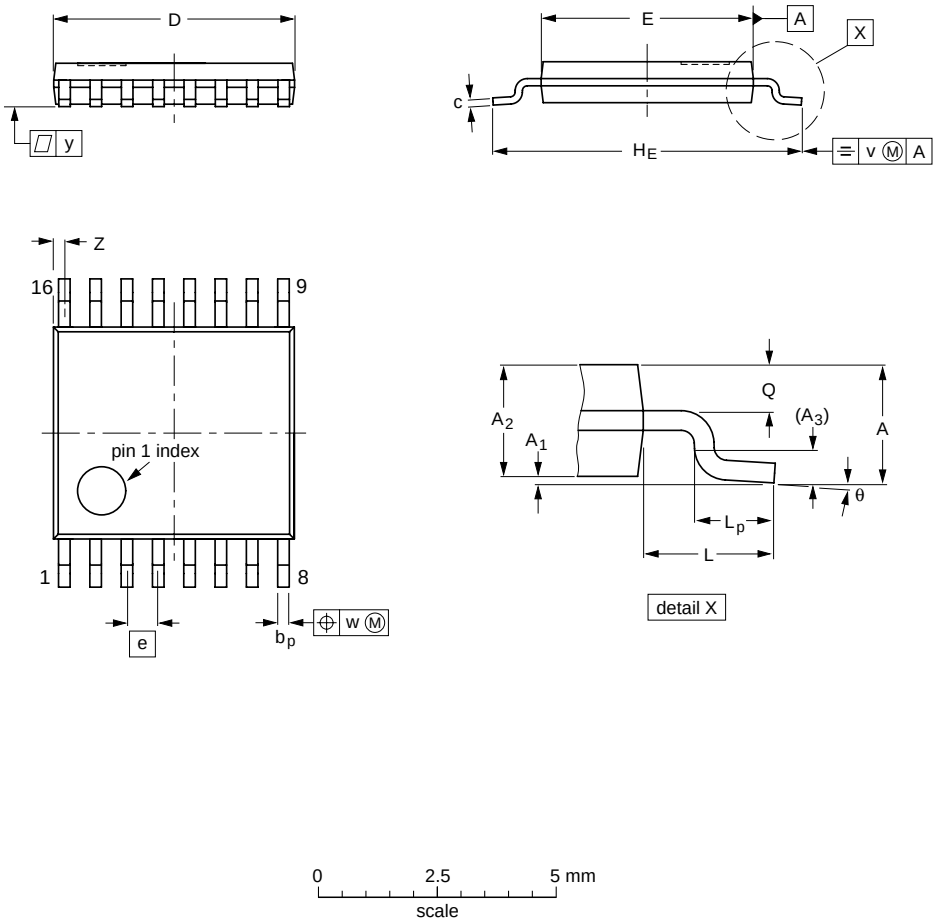
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT109-1 | 076E07 | MS-012 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 17. Package outline SOT109-1 (SO16)**


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**TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm** **SOT403-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (2) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1 | 0.15<br>0.05 | 0.95<br>0.80 | 0.25 | 0.30<br>0.19 | 0.2<br>0.1 | 5.1<br>4.9 | 4.5<br>4.3 | 0.65 | 6.6<br>6.2 | 1 | 0.75<br>0.50 | 0.4<br>0.3 | 0.2 | 0.13 | 0.1 | 0.40<br>0.06 | $8^o$<br>$0^o$ |

**Notes**

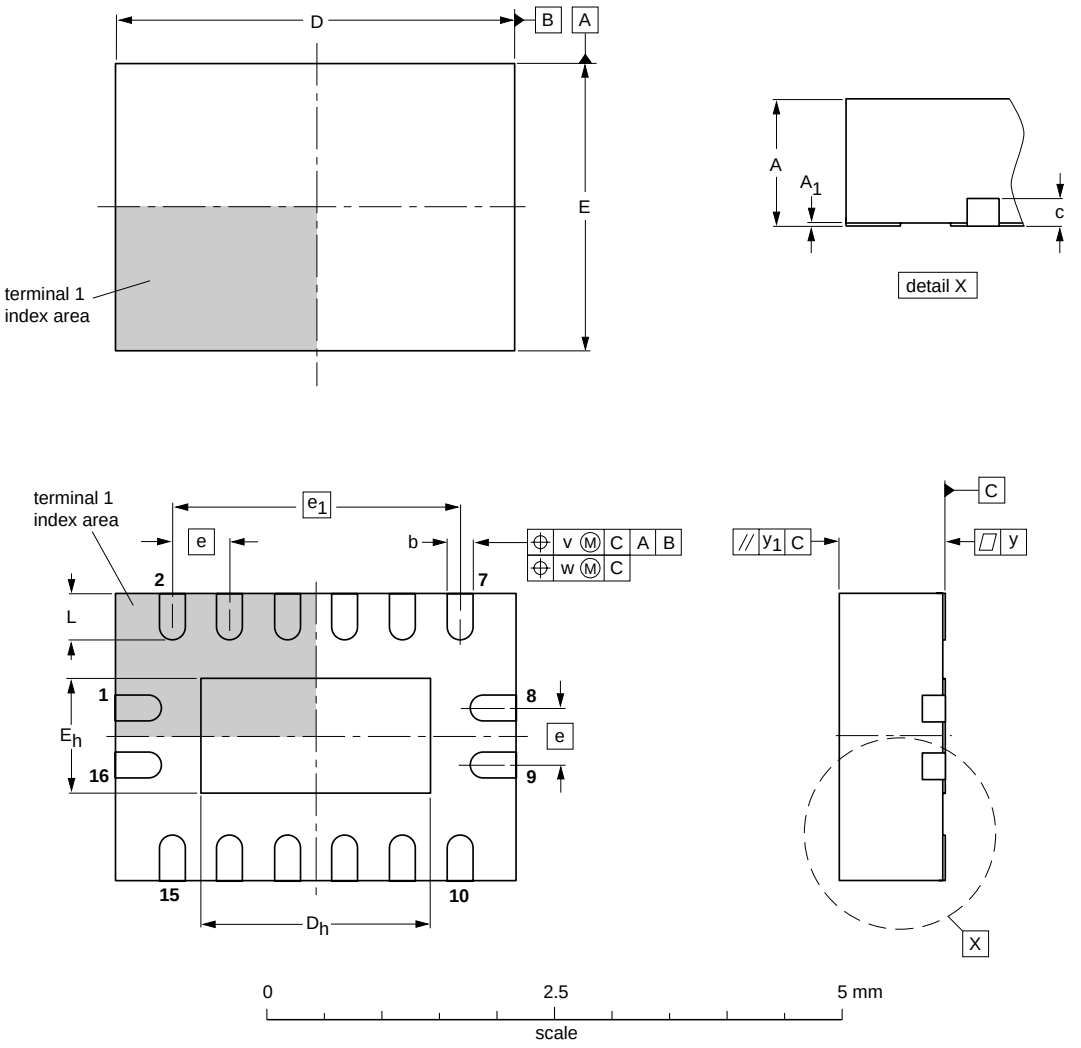
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT403-1 | | MO-153 | | | | ~~99-12-27~~<br>03-02-18 |

**Fig 18. Package outline SOT403-1 (TSSOP16)**


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**DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm** **SOT763-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A(1) max. | $A_1$ | b | c | D(1) | $D_h$ | E(1) | $E_h$ | e | $e_1$ | L | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1 | 0.05<br>0.00 | 0.30<br>0.18 | 0.2 | 3.6<br>3.4 | 2.15<br>1.85 | 2.6<br>2.4 | 1.15<br>0.85 | 0.5 | 2.5 | 0.5<br>0.3 | 0.1 | 0.05 | 0.05 | 0.1 |

**Note**

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT763-1 | - - - | MO-241 | - - - | | | ~~02-10-17~~<br>03-01-27 |

**Fig 19. Package outline SOT763-1 (DHVQFN16)**


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## 13. Abbreviations

Table 10. Abbreviations

| Acronym | Description |
|---|---|
| CDM | Charged Device Model |
| CMOS | Complementary Metal-Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

## 14. Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| 74HC590_2 | 20090428 | Product data sheet | - | 74HC590_1 |
| Modifications: | • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.<br>• Legal texts have been adapted to the new company name where appropriate.<br>• Quick reference data incorporated in to Section 9 and Section 10.<br>• Added type number 74HC590N (DIP16 package) | | | |
| 74HC590_1 | 20050330 | Product data sheet | - | - |


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# 15. Legal information

## 15.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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